What is claimed is:

1. A gate stack for a nonvolatile memory cell, comprising:

a Silicon Dioxide (SiO_2) layer in contact with a channel region of the memory cell;

a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer;

a charge-storage region in contact with the Ta_2O_5 layer; and

a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer.

2. The gate stack of claim 1, wherein the SiO_2 layer includes approximately 2 nm of NH_3 treated SiO_2.

3. The gate stack of claim 1, wherein the SiO_2 layer includes approximately 2 nm of NO treated SiO_2.

4. The gate stack of claim 1, wherein the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5.

5. The gate stack of claim 1, wherein the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

6. The gate stack of claim 1, wherein:

the SiO_2 layer includes approximately 2 nm of SiO_2;

the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5; and

the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

7. The gate stack of claim 1, wherein the floating charge-storage region includes a silicon floating gate.

8. A gate stack for a nonvolatile memory cell, comprising:

a Silicon Dioxide (SiO_2) layer in contact with a channel region of the memory cell;

a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer;

a charge-trapping floating plate in contact with the Ta_2O_5 layer; and

a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer.

9. The gate stack of claim 8, wherein the floating plate includes Silicon-Rich-Oxide (SRO).

10. The gate stack of claim 9, wherein the SRO has a refractive index of approximately 1.6.

11. The gate stack of claim 8, wherein the floating plate includes Silicon Rich-Nitride (SRN).

12. The gate stack of claim 11, wherein the SRN has a refractive index of approximately 2.2.

13. The gate stack of claim 8, further comprising an injector SRN layer disposed between a control gate and the ZrO_2 layer.

14. The gate stack of claim 8, further comprising an injector SRN layer disposed between the SiO_2 layer and the Ta_2O_5 layer.

15. The gate stack of claim 8, further comprising an injector SRN layer disposed between the SiO_2 layer and the Ta_2O_5 layer and an injector SRN layer disposed between a control gate and the ZrO_2 layer.

16. A nonvolatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a control gate of predetermined metallurgy; and

a gate stack separating the control gate from the channel region, the gate stack including:

a first insulator region including a Silicon Dioxide (SiO_2) layer and a Tantalum Oxide (Ta_2O_5) layer;

a floating charge-storage region separated from the channel region by the first insulator region; and

a second insulator region including a Zirconium Oxide (ZrO_2) layer, wherein the control gate is separated from the floating charge-storage region by the second insulator region;

wherein the gate stack includes selected material for providing desired asymmetric energy barriers in conjunction with the control gate of predetermined metallurgy, and

wherein the desired asymmetric energy barriers are adapted to:

primarily restrict carrier flow during programming to a selected carrier between the control gate and the floating charge-storage region, and

retain a programmed charge in the floating charge-storage region.

17. The nonvolatile memory cell of claim 16, wherein the asymmetric energy barriers include a hole energy barrier from the control gate to the floating charge-storage region that is adapted to promote hole transport from the control gate to the floating charge-storage region during a first programming operation.

18. The nonvolatile memory cell of claim 17, wherein the asymmetric energy barriers include an electron energy barrier from the floating charge-storage region that is adapted to promote complementary electron transport from the floating charge-storage region to the control gate during a first programming operation.

19. The nonvolatile memory cell of claim 17, wherein the asymmetric energy barriers include:

a hole energy barrier from the floating charge-storage region to the substrate and a hole energy barrier from the floating charge-storage region to the control gate that are adapted to retain holes transported from the control gate during the first programming operation as the programmed charge in the floating charge-storage region; and

an electron energy barrier from the substrate to the floating charge-storage region and an electron energy barrier from the control gate to the floating charge-storage region that are adapted to restrict electron emissions from the substrate and from the control gate into the floating charge-storage region to a negligible amount of electrons.

20. The nonvolatile memory cell of claim 16, wherein the floating charge-storage region includes a silicon floating gate.

21. The nonvolatile memory cell of claim 16, wherein the floating charge-storage region includes a charge-trapping floating plate.

22. The nonvolatile memory cell of claim 16, wherein the first insulator region includes a Silicon Dioxide (SiO_2) layer in contact with the channel region and a Tantalum Oxide (Ta_2O_5) layer disposed between the SiO_2 layer and the floating charge-storage region.

23. The nonvolatile memory cell of claim 16, wherein the second insulator region includes a Zirconium Oxide (Zr_2O_5) layer.

24. The nonvolatile memory cell of claim 16, further comprising an Oxide-Nitride-Oxide (ONO) gate stack sidewall.

25. A nonvolatile memory cell, comprising:

a p – substrate;

a first n type source/drain region and a second n type source/drain region separated by a channel region in the substrate;

a Silicon Dioxide (SiO_2) layer in contact with the channel region;

a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer;

a charge-storage region in contact with the Ta_2O_5 layer;

a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer; and

an Aluminum control gate in contact with the ZrO_2 layer.

26. The nonvolatile memory cell of claim 25, wherein the SiO_2 layer includes approximately 2 nm of NH_3 treated SiO_2.

27. The nonvolatile memory cell of claim 25, wherein the SiO_2 layer includes approximately 2 nm of NO treated SiO_2.

28. The nonvolatile memory cell of claim 25, wherein the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5.

29. The nonvolatile memory cell of claim 25, wherein the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

30. The nonvolatile memory cell of claim 25, wherein the first n type source/drain region and the second n type source/drain region both include an n – diffusion region and an n + diffusion region.

31. The nonvolatile memory cell of claim 25, wherein:
the SiO_2 layer includes approximately 2 nm of SiO_2;
the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5; and
the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

32. The nonvolatile memory cell of claim 25, wherein the floating charge-storage region includes a silicon floating gate.

33. The nonvolatile memory cell of claim 25, wherein the floating charge-storage region includes a charge-trapping floating plate.

34. A nonvolatile memory cell, comprising:
a first source/drain region and a second source/drain region separated by a channel region in a substrate;
a control gate of predetermined metallurgy;
a gate stack separating the control gate from the channel region, the gate stack including:
a first insulator region including a Silicon Dioxide (SiO_2) layer and a Tantalum Oxide (Ta_2O_5) layer;
a floating plate separated from the channel region by the first insulator region, the floating plate including silicon nano crystals; and

a second insulator region including a Zirconium Oxide (ZrO_2) layer,

wherein the control gate is separated from the floating charge-storage region by the second insulator region;

wherein the gate stack includes selected material for providing desired asymmetric energy barriers in conjunction with the predetermined metallurgy of the control gate, and

wherein the desired asymmetric energy barriers are adapted to:

primarily restrict carrier flow during programming to a selected carrier between the control gate and the floating charge-storing region, and

retain a programmed charge in the floating charge-storage region.

35. The nonvolatile memory cell of claim 34, wherein the floating plate includes Silicon-Rich-Oxide (SRO).

36. The nonvolatile memory cell of claim 35, wherein the SRO has a refractive index of approximately 1.6.

37. The nonvolatile memory cell of claim 34, wherein the floating plate includes Silicon Rich-Nitride (SRN).

38. The nonvolatile memory cell of claim 37, wherein the SRN has a refractive index of approximately 2.2.

39. The nonvolatile memory cell of claim 34, wherein the second insulator region includes a Zirconium Oxide (ZrO_2) layer, further comprising an injector SRN layer disposed between the control gate and the ZrO_2 layer.

40. The nonvolatile memory cell of claim 34, wherein the first insulator region includes a silicon dioxide (SiO_2) layer in contact with the channel region and a Tantalum Oxide (Ta_2O_5) layer disposed between the SiO_2 layer and the floating plate, further comprising an injector SRN layer disposed between the SiO_2 layer and the Ta_2O_5 layer.

41. The nonvolatile memory cell of claim 34, wherein:

the first insulator region includes a silicon dioxide (SiO_2) layer in contact with the channel region and a Tantalum Oxide (Ta_2O_5) layer disposed between the SiO_2 layer and the floating plate;

the second insulator region includes a Zirconium Oxide (ZrO_2) layer; and

the memory further comprises an injector SRN layer disposed between the SiO_2 layer and the Ta_2O_5 layer and an injector SRN layer disposed between the control gate and the ZrO_2 layer.

42. A nonvolatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a control gate; and

a gate stack separating the control gate from the channel region, the gate stack including:

a first insulator region;

a floating charge-storage region separated from the channel region by the first insulator region; and

a second insulator region, wherein the control gate is separated from the floating charge-storage region by the second insulator region,

wherein a hole energy barrier from the control gate to the second insulator region is sufficiently small such that a primary programming charge transport includes hole transport from the control gate to the floating charge-storage region upon application of a programming electromotive force (EMF) at the control gate that is positive with respect to the substrate.

43. The nonvolatile memory cell of claim 42, wherein the hole energy barrier from the control gate to the second insulator region is approximately 1.9 ev.

44. The nonvolatile memory cell of claim 42, wherein an electron energy barrier from the substrate to the first insulator region is such that electron transport from the substrate to the floating charge-storage region is discouraged when applying the programming EMF at the control gate that is positive with respect to the substrate.

45. The nonvolatile memory cell of claim 44, wherein the electron energy barrier from the substrate to the first insulator region is approximately 3.2 ev.

46. The nonvolatile memory cell of claim 42, wherein an electron energy barrier from the floating charge-storage region to the second insulator region is such that a complimentary charge transport that further enhances programming speed includes electron transport from the floating charge-storage region to the control gate upon application of the programming EMF at the control gate that is positive with respect to the substrate.

47. The nonvolatile memory cell of claim 46, wherein the electron energy barrier from the floating charge-storage region to the second insulator region is approximately 1.5 ev.

48. The nonvolatile memory cell of claim 42, wherein an electron energy barrier from the floating charge-storage region to the first insulator region is such that electron transport from the floating charge-storage region to the substrate is small if an EMF transient is present at the substrate that is positive with respect to the floating charge-storage region.

49. The nonvolatile memory cell of claim 48, wherein the electron energy barrier from the floating charge-storage region to the first insulator region is a composite electron energy barrier of approximately 3.2 ev.

50. The nonvolatile memory cell of claim 42, wherein:

a hole energy barrier from the floating charge-storage region to the first insulator region and a hole energy barrier from the floating charge-storage region to the second insulator region is such that, upon removing the programming EMF, hole emission from the floating charge-storage region is negligible; and

an electron energy barrier from the substrate to the first insulator region and an electron energy barrier from the control gate to the second insulator region is such that, upon removing the programming EMF, electron emission from the floating charge-storage region to the control gate and to the substrate is negligible.

51. The nonvolatile memory cell of claim 50, wherein:

the hole energy barrier from the floating charge-storage region to the first insulator region is approximately 2.9 ev with an additional energy barrier of approximately 1.8 ev for a composite energy barrier of approximately 4.7 ev;

the hole energy barrier from the floating charge-storage region to the second insulator region is approximately 3.1 ev;

the electron energy barrier from the substrate to the first insulator region is approximately 3.2 ev; and

the electron energy barrier from the control gate to the second insulator region is approximately 3.8 ev.

52. The nonvolatile memory cell of claim 42, wherein the programming electromotive force (EMF) at the control gate that is positive with respect to the substrate is approximately 12 V.

53. The nonvolatile memory cell of claim 42, wherein:

the floating charge-storage region includes a floating plate with silicon nano crystals; and

the programming electromotive force (EMF) at the control gate that is positive with respect to the substrate is approximately 9 V.

54. A nonvolatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a control gate; and

a gate stack separating the control gate from the channel region, the gate stack including:

a first insulator region;

a floating charge-storage region separated from the channel region by the first insulator region; and

a second insulator region, wherein the control gate is separated from the floating charge-storage region by the second insulator region,

wherein a hole energy barrier from the floating charge-storage region to the second insulator region and the equivalent oxide thicknesses of the second insulator region and the first insulator region are such that hole transport from the floating

charge-storage region to the control gate is encouraged if an EMF transient is present at the substrate that is positive with respect to the control gate.

55. The nonvolatile memory cell of claim 54, wherein the hole energy barrier from the floating charge-storage region to the second insulator region is approximately 3.1 ev.

56. The nonvolatile memory cell of claim 54, wherein an electron energy barrier from the control gate to the second insulator region is such that a complimentary charge transport to further enhance programming speed includes electron transport from the control gate to the floating charge-storage region if an EMF transient is present at the substrate that is positive with respect to the control gate.

57. The nonvolatile memory cell of claim 56, wherein the electron energy barrier from the control gate to the second insulator region is approximately 3.8 ev.

58. The nonvolatile memory cell of claim 54, wherein a hole energy barrier from the substrate to the first insulator region is such that hole transport from the substrate is negligible if a programming EMF is present at the substrate that is positive with respect to the control gate.

59. The nonvolatile memory cell of claim 58, wherein the hole energy barrier from the substrate to the first insulator region is approximately 4.7 ev.

60. The nonvolatile memory cell of claim 54, wherein an electron energy barrier from the floating charge region to the first insulator region is such that an effective electron transport from the floating charge-storage region to the substrate through field emission is small if a programming EMF is present at the substrate that is positive with respect to the control gate.

61. The nonvolatile memory cell of claim 60, wherein the electron energy barrier from the floating charge-storing region to the first insulator region is a composite electron energy barrier of approximately 3.2 ev.

62. The nonvolatile memory cell of claim 54, wherein the programming EMF is present at the substrate that is positive with respect to the control gate by approximately +12 V.

63. The nonvolatile memory cell of claim 54, wherein:

the floating charge-storage region includes a floating plate with silicon nano crystals; and

the programming EMF is present at the substrate that is positive with respect to the control gate is approximately +9 V.

64. A nonvolatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a control gate; and

a gate stack separating the control gate from the channel region, the gate stack including:

a first insulator region having a first equivalent oxide thickness;

a floating charge-storage region separated from the channel region by the first insulator region; and

a second insulator region having a second equivalent oxide thickness, wherein the control gate is separated from the floating charge-storage region by the second insulator region,

wherein the equivalent oxide thickness of the first insulator region and the equivalent oxide thickness of the second insulator region is such that an electric field across the second insulator region is enhanced when a programming potential is applied across the control gate and the substrate,

wherein the first insulator region and the second insulator region include materials that provide desired asymmetric energy barriers, and

wherein the desired asymmetric energy barriers are adapted to:

primarily restrict carrier flow during programming to a selected carrier between the control gate and the floating charge-storage region, and

retain a programmed charge in the floating charge-storage region.

65. The nonvolatile memory cell of claim 64, wherein the selected carrier between the control gate and the floating charge-storage gate includes holes.

66. The nonvolatile memory cell of claim 64, wherein:

the substrate includes p – silicon;

the first insulator region includes a Silicon Dioxide (SiO_2) layer in contact with the channel region and a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer and with the charge-storage region;

the second oxide includes a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer; and

the control gate includes aluminum.

67. The nonvolatile memory cell of claim 66, wherein:

the SiO_2 layer includes approximately 2 nm of SiO_2;

the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5; and

the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

68. A flash memory array, comprising:

a number of nonvolatile memory cells, wherein each nonvolatile memory cell includes:

a p – substrate;

a first n type source/drain region and a second n type source/drain region separated by a channel region in the substrate;

a Silicon Dioxide (SiO_2) layer in contact with the channel region;

a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer;

a charge-storage region in contact with the Ta_2O_5 layer;

a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer; and

an Aluminum control gate in contact with the ZrO_2 layer;

a number of source lines, each of the source lines being coupled to the first source/drain region of at least one of the memory cells;

a number of control gate lines, each of the gate lines being coupled to the control gate of at least one of the memory cells; and

a number of bit lines, each of the bit lines being coupled to the second source/drain region of at least one of the memory cells.

69. The flash memory array of claim 68, wherein the SiO_2 layer includes approximately 2 nm of NH_3 treated SiO_2.

70. The flash memory array of claim 68, wherein the SiO_2 layer includes approximately 2 nm of NO treated SiO_2.

71. The flash memory array of claim 68, wherein the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5.

72. The flash memory array of claim 68, wherein the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

73. The flash memory array of claim 68, wherein the first n type source/drain region and the second n type source/drain region both include an n – diffusion region and an n + diffusion region.

74. The flash memory array of claim 68, wherein:
the SiO_2 layer includes approximately 2 nm of SiO_2;
the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5; and
the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

75. The flash memory array of claim 68, wherein the floating charge-storage region includes a silicon floating gate.

76. The flash memory array of claim 68, wherein the floating charge-storage region includes a charge-trapping floating plate.

77. An electronic system, comprising:

a processor; and

a memory device adapted to communicate with the processor, wherein the memory device includes an array of flash memory cells, comprising:

a number of nonvolatile memory cells, wherein each nonvolatile memory cell includes:

a p – substrate;

a first n type source/drain region and a second n type source/drain region separated by a channel region in the substrate;

a Silicon Dioxide (SiO_2) layer in contact with the channel region;

a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer;

a charge-storage region in contact with the Ta_2O_5 layer;

a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer; and

an Aluminum control gate in contact with the ZrO_2 layer;

a number of source lines, each of the source lines being coupled to the first source/drain region of at least one of the memory cells;

a number of control gate lines, each of the gate lines being coupled to the control gate of at least one of the memory cells; and

a number of bit lines, each of the bit lines being coupled to the second source/drain region of at least one of the memory cells.

78. The electronic system of claim 77, wherein:

the SiO_2 layer includes approximately 2 nm of SiO_2;

the Ta_2O_5 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5; and

the ZrO_2 layer includes approximately 3 - 5 nm $t_{ox.eq.}$ of ZrO_2.

79. A method of forming a floating gate transistor, comprising:

forming a first source/drain region and a second source/drain region separated by a channel region in a p – substrate;

forming a gate stack over the channel region, including:

forming an SiO_2 layer on the channel region;

forming a Ta_2O_5 layer on the SiO_2 layer;

forming a floating charge-storage region on the Ta_2O_5 layer; and

forming a ZrO_2 layer on the floating charge-storage region; and

forming an aluminum control gate on the Ta_2O_5 layer.

80. The method of forming a floating gate transistor of claim 79, wherein forming an SiO_2 layer on the channel region includes forming an approximately 2 nm thick layer of SiO_2.

81. The method of forming a floating gate transistor of claim 79, wherein forming a Ta_2O_5 layer on the SiO_2 layer includes forming a layer of Ta_2O_5 that has an equivalent oxide thickness of approximately 3 to 5 nm.

82. The method of forming a floating gate transistor of claim 79, wherein forming a floating charge-storage region on the Ta_2O_5 layer includes forming a silicon floating gate.

83. The method of forming a floating gate transistor of claim 79, wherein forming a floating charge-storage region on the Ta_2O_5 layer includes forming a floating plate with silicon nano crystals.

84. The method of forming a floating gate transistor of claim 79, wherein forming a ZrO_2 layer on the floating charge-storage region includes forming a layer of ZrO_2 that has an equivalent oxide thickness of approximately 3 to 5 nm.

85. A method for operating a nonvolatile memory cell, comprising:

erasing the nonvolatile memory cell from the high threshold nonconducting state (1) to the low threshold conducting state (0) by applying a positive programming pulse to a control gate of the cell while pulling a substrate of the cell to a ground potential, wherein the positive programming pulse induces an erase primary charge transport of holes from the control gate to a floating charge-storage region of the cell; and

writing the nonvolatile memory cell from a low threshold conducting state (0) to a high threshold nonconducting state (1) by applying a positive programming pulse to a drain node to capacitively pull the substrate of the cell to a positive potential while pulling the control gate of the cell to a ground potential, wherein the positive programming pulse induces a write primary charge transport of holes from the floating charge-storage region of the cell to the control gate.

86. The method of claim 85, wherein both the positive programming pulse applied at the control gate to erase the nonvolatile memory cell and the positive programming pulse applied at the drain node to write the nonvolatile memory cell includes a 10 msec. + 12 V pulse .

87. The method of claim 85, wherein both the positive programming pulse applied at the control gate to erase the nonvolatile memory cell and the positive programming pulse applied at the drain node to write the nonvolatile memory cell includes a 10 msec. + 9 V pulse.

88. The method of claim 85, further comprising reading the nonvolatile memory cell by:

applying approximately 2.5 V to a drain and to the control gate of the memory cell;

pulling the substrate of the memory cell and a source of the memory cell to ground; and

sensing drain current to determine if the memory cell is in a high threshold nonconducting state to a low threshold conducting state.